IN THE CLAIMS:

Claims 1-13 (Canceled)

Claim 14 (currently amended): A method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) providing a substrate, ~~placing semiconductor chip on an upper surface of a substrate, said substrate having the~~

an upper surface of the substrate including a first region and a second region, the first region including ~~on which a first~~ an upper metal pattern [[is]] formed thereon and the second region including at least one registration mark,

a lower surface of the substrate including ~~on which~~ a ~~second~~ lower metal pattern [[is]] formed thereon, said ~~first~~ upper metal pattern and ~~second~~ said lower metal pattern being electrically connected to each other through said substrate;

(b) providing a semiconductor chip;

(c) placing said semiconductor chip on the upper surface of said substrate within the first region;

(d) electrically connecting the semiconductor chip and the ~~first~~ upper metal pattern to each other;

[[(c)]] (e) sealing the semiconductor chip and the ~~first~~ upper metal pattern with sealing resin, the sealing resin covering the first region but not the second region, whereby the registration mark is not covered by the resin; and

[[(d)]] (f) forming, in the first region and through the sealing resin, a through hole which reaches the ~~first~~ upper metal pattern by using the registration mark to align the through hole to the upper metal pattern; [[,]] and

(g) forming a wire inside the through hole to electrically connect to the ~~first~~ upper metal pattern.

Claim 15 (currently amended): [[A]] The method according to claim 14, wherein the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin.

Claim 16 (currently amended): A method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) preparing a substrate having an upper surface and a lower surface, the upper surface of the substrate including a first region and a second region, the second region including at least one registration mark;

(b) forming ~~a first~~ an upper metal pattern on an upper surface of the substrate;

(c) forming a ~~second~~ lower metal pattern on a lower surface of the substrate;

(d) electrically connecting the ~~first~~ upper metal pattern and the ~~second~~ lower metal pattern to each other;

(e) placing a semiconductor chip on the upper surface of the substrate;

(f) electrically connecting the semiconductor chip and the ~~first~~ upper metal pattern to each other;

(g) sealing the semiconductor chip and the ~~first~~ upper metal pattern with sealing resin, the sealing resin covering the first region but not the second region, whereby the registration mark is not covered by the resin;

(h) forming, in the first region and through the sealing resin, a through hole extending from the surface of the sealing resin to the ~~first~~ upper metal pattern by using the registration mark to align the through hole to the upper metal pattern; and

(i) forming a wire inside the through hole.

Claim 17 (currently amended): [[A]] The method according to claim 16, wherein the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin.

Claim 18 (currently amended): [[A]] The method according to claim 14, further comprising:

(a) disposing a second substrate on the sealing resin after forming the wire inside the through hole; and

(b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other.

Claim 19 (currently amended): [[A]] The method according to claim 14, wherein said placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising:

separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole.

Claim 20 (currently amended): [[A]] The method according to claim 14, further comprising:

(a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire;

(b) forming an insulating layer on the fourth wire; and

(c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.

Claim 21 (currently amended): [[A]] The method according to claim 16, further comprising:

(a) disposing a second substrate on the sealing resin after forming the wire inside the through hole; and

(b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other.

Claim 22 (currently amended): [[A]] The method according to claim 16, wherein said placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising:

separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole.

Claim 23 (currently amended): [[A]] The method according to claim 16, further comprising:

(a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire;

(b) forming an insulating layer on the fourth wire; and

(c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.

Claim 24 (new): The method according to claim 14, comprising forming the registration mark along with the upper metal pattern.

Claim 25 (new): The method according to claim 16, comprising forming the registration mark along with the upper metal pattern.

Claim 26 (new): The method according to claim 14,

wherein the step of placing said semiconductor chip on the upper surface of said substrate within the first region includes placing a plurality of the semiconductor chip on a single substrate;

wherein the plural semiconductor chips are deployed on the substrate in a rectangular array within the first region; and

wherein the step of providing the substrate includes forming the registration mark within the second region at a corner of the array.

Claim 27 (new): The method according to claim 16,

wherein the step of placing said semiconductor chip on the upper surface of said substrate within the first region includes placing a plurality of the semiconductor chip on a single substrate;

wherein the plural semiconductor chips are deployed on the substrate in a rectangular array within the first region; and

wherein the step of providing the substrate includes forming the registration mark within the second region at a corner of the array.